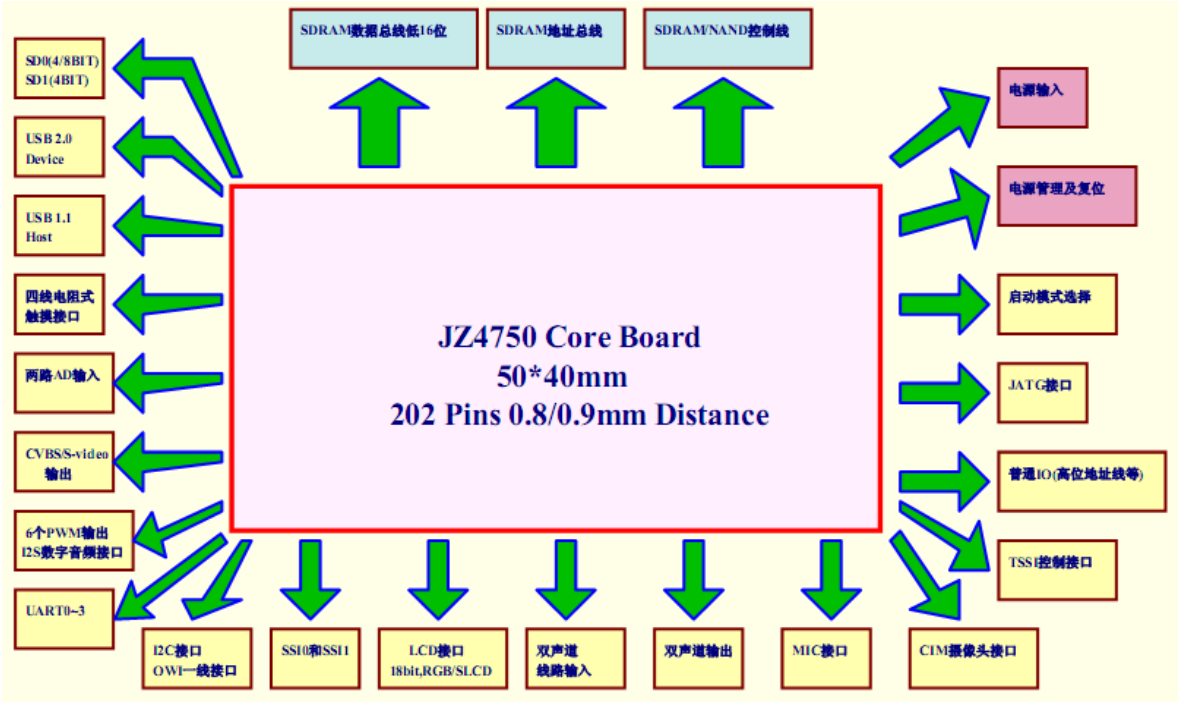
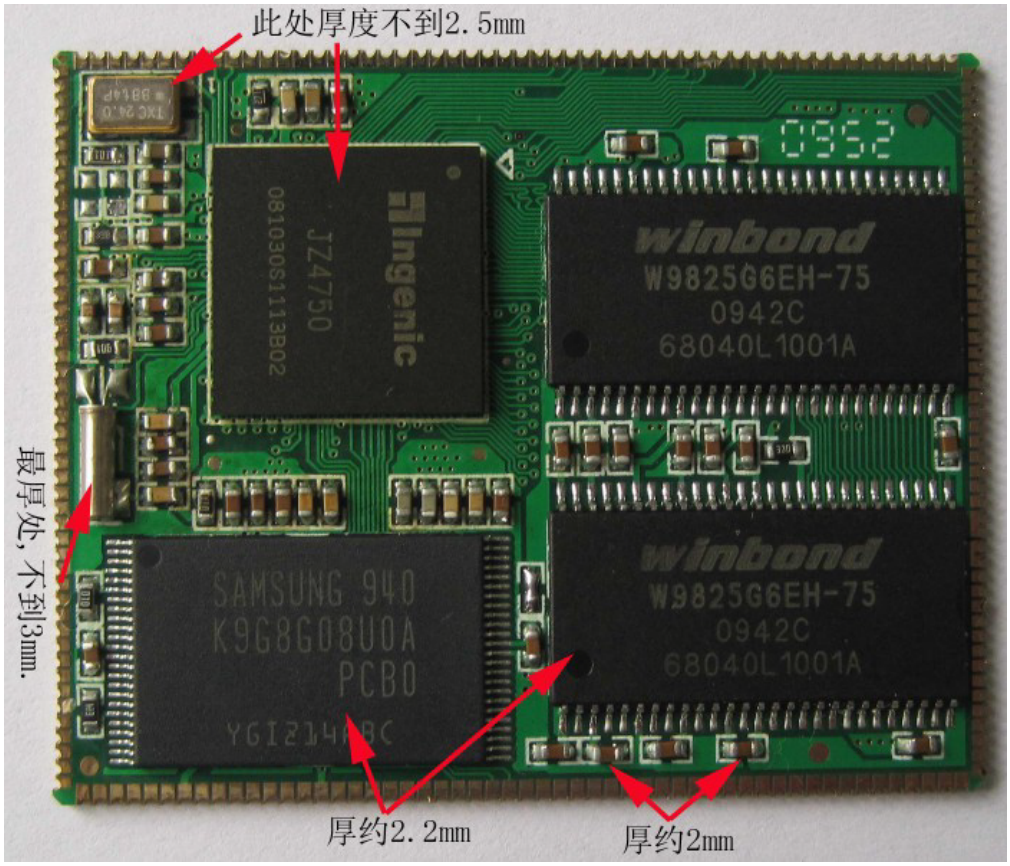
JZ4750 核心板说明

总述：

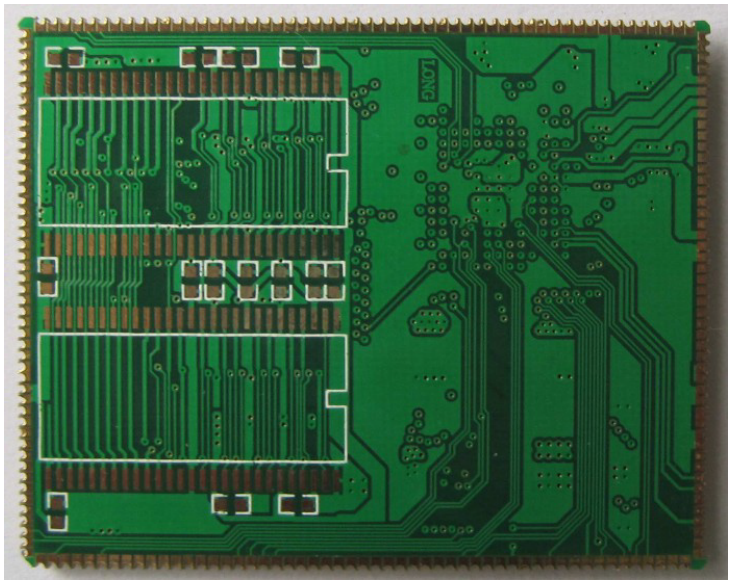
JZ4750 核心板上包括 4 片 SDRAM，一片 NAND FLASH，一颗 JZ4750 芯片，还有周边配套的电阻电容元件，以及晶振电路。它引出的接口大致如下：



它总共有 202 个 PIN，最大外形尺寸为 50*40mm，PCB 板厚度 1.00mm(样板为 1.2mm)，加上各元件的总厚度如下图所示：



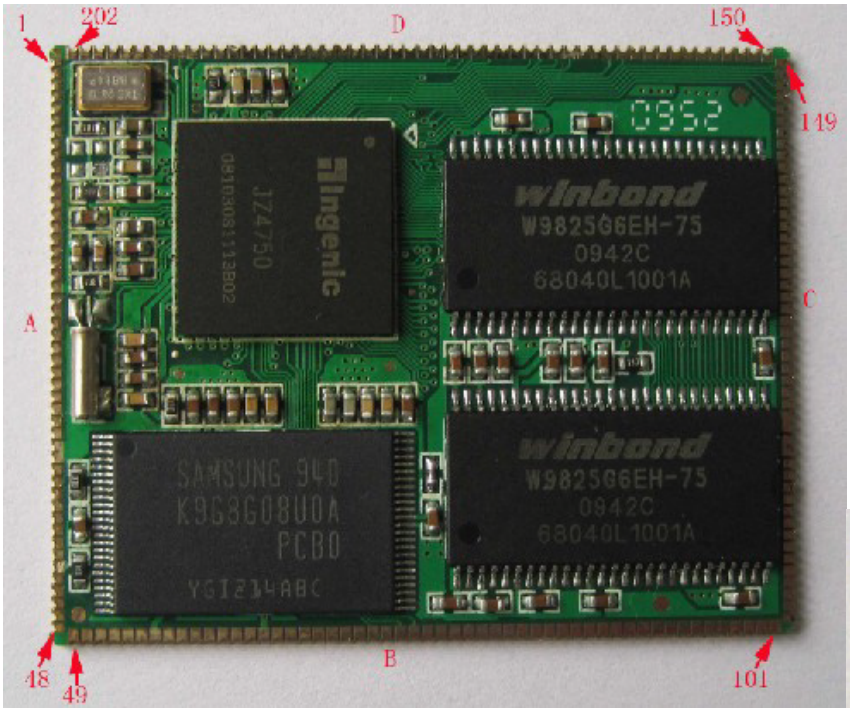
本核心板是四层玻纤板(FR-4)，默认配置是 64M SDRAM，1G NAND(型号是 K9G8G08U0A)，核心板支持 128M SDRAM，背面还可以焊上两片 32M 的 SDRAM，如下图：

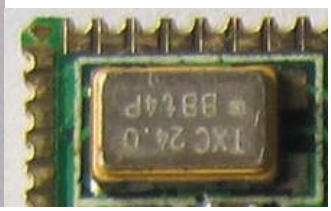


这里背面的 0603 元件均为 0.1uF 电容。如果你焊上了背面 SDRAM，底板的设计上应该在相应的位置上挖出孔来，这个孔的位置我有做在“JZ4750-CORE 应用”中的 PCB 封装中，可以参考使用。

引脚说明：

JZ4750 核心板共 202 个引脚，位于左上角(四方形晶振处)有一个小小的三角形标识，它指向核心板的第一脚，其它引脚数以逆时针累加。





上图中的 A 区及 C 区为 48 个 PIN，其引脚间距为 0.8MM；B 区与 D 区为 53 个 PIN，其引脚间距为 0.9MM。这个核心板应用的 SCH 及 PCB 封装我也都做好了，目前是 Protel 99se 格式的封装。

JZ4750 核心板引脚排列表：

Num	Pin	IO	IO Cell	PinDescription	Power
1	UART1_RTS_ PCM_DOUT PE19	O O IO	2mA, Pullup-pe	UART1_RTS_: UART 1 RTS_ output PCM_DOUT: PCM data output PE19: GPIO group E bit 19	VDDIO
2	UART1_CTS_ PCM_DIN PE18	I I IO	2mA, Pullup-pe	UART1_CTS_: UART 1 CTS_ input PCM_DIN: PCM data input PE18: GPIO group E bit 18	VDDIO
3	PWM0 PCM_CLK PE20	O IO IO	2mA, Pullup-pe	PWM0: PWM 0 output PCM_CLK: PCM clock PE20: GPIO group E bit 20	VDDIO
4	PWM1 PCM_SYN PE21	O IO IO	2mA, Pullup-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PCM_SYN: PCM sync PE21: GPIO group E bit 21	VDDIOL
5	VDDPLL	P		VDDPLL: PLL analog power, 1.8V	-
6	GND	P		VSSPLL: PLL analog ground	-
7	VDDADC	P		AVDAD: ADC analog power, 3.3 V	-
8	GND	P		AVDAD: ADC analog ground	-
9	XN	AI		XN: Touch screen X- input	AVDAD
10	XP	AI		XP: Touch screen X+ input	AVDAD
11	YP	AI		YP: Touch screen Y+ input	AVDAD
12	YN	AI		YN: Touch screen Y- input	AVDAD
13	ADIN1	AI		ADIN1: ADC general purpose input 1	AVDAD
14	PBAT/ADIN0	AI		ADIN0: Battery voltage input or ADC general purpose input 0	AVDAD
15	DM0	AIO		DM0: USB 2.0 device data minus	AVDUSB
16	DP0	AIO		DP0: USB 2.0 device data plus	AVDUSB
17	DM1	AIO		DM1: USB 1.1 host data minus	AVDUSB
18	DP1	AIO		DP1: USB 1.1 host data plus	AVDUSB
19	VDD_USB	P		AVDUSB: USB analog power, 3.3V	-
20	GND	P		AVSUSB: USB analog ground	-
21	GND	P		Power, ground	-
22	VRTC	P		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-
23	PWRON	AO	~2mA, open-drain	PWRON_: Power on/off control of main power	VDDRTC
24	PPRST	AI	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC
25	WKUP_ PE30	AI AI	Schmitt	WKUP_: Wake signal after main power down PE30: GPIO group E bit 30, input/interrupt only	VDDRTC
26	TDI UART2_RxD	I I	Schmitt, pullup-pe	TDI: JTAG serial data input UART2_RxD: UART 2 Receiving data, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
27	TDO	O	4mA	TDO: JTAG serial data output	VDDIO

	UART2_TxD	O		UART2_TxD: UART 2 transmitting data, PE31 is used to select between JTAG and UART, reset to JTAG	
28	TRST_	I	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
29	TMS UART2_CTS	I I	Schmitt, pullup-pe	TMS: JTAG mode select UART2_CTS_: UART 2 CTS_ input, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
30	TCK UART2_RTS	I O	2mA, Schmitt, pulldown-pe	TCK: JTAG clock UART2_RTS_: UART 2 RTS_ output, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
31	VDD	P		power, 3.3V	-
32	VDD	P		power, 3.3V	-
33	GND	P		power, ground	-
34	GND	P		power, ground	-
35	VDD_CORE	P		VDDCORE: CORE digital power, 1.8V	-
36	VDD_CORE	P		VDDCORE: CORE digital power, 1.8V	-
37	GND	P		VSSCORE: CORE digital ground	-
38	GND	P		VSSCORE: CORE digital ground	-
39	MICP	AI		MICP: Microphone input	AVDHP
40	MICBIAS	AO		MICBIAS: Microphone bias	AVDHP
41	AIR	AI		AIR: Right line input	AVDHP
42	AOHPMS	AI		HPCMSI: Headphone common mode sense input	AVDHP
43	AIL	AI		AIL: Left line input	AVDHP
44	AOHPR	AO		AOHPR: Right headphone out	AVDHP
45	AOHPM	AO		HPCMO: Headphone common mode output	AVDHP
46	AOHPL	AO		AOHPL: Left headphone out	AVDHP
47	SSI0_CLK PB26	O IO	4mA, pullup-pe	SSI0_CLK: SSI 0 clock output PB26: GPIO group B bit 26	VDDIO
48	SSI0_DR PB28	I IO	4mA, pullup-pe	SSI0_DR: SSI 0 data input PB28: GPIO group B bit 28	VDDIO
49	SSI0_DT PB27	O IO	4mA, pullup-pe	SSI0_DT: SSI 0 data output PB27: GPIO group B bit 27	VDDIO
50	SSI0_CE0_ PB29	O IO	4mA, pullup-pe	SSI0_CE0_: SSI 0 chip enable 0 PB29:GPIO group B bit 29	VDDIO
51	SSI0_CE1_ PB31	O IO	4mA, pullup-pe	SSI0_CE1_: SSI 0 chip enable 1 PB31: GPIO group B bit 31	VDDIO
52	SSI0_GPC PB30	O IO	4mA, pullup-pe	SSI0_GPC: SSI 0 general-purpose control signal PB30: GPIO group B bit 30	VDDIO
53	SDATI UART2_RxD PE27	I I IO	2mA, pullup-pe	SDATI: AC97/I2S serial data input UART2_RxD: UART 2 Receiving data PE27: GPIO group E bit 27	VDDIO
54	SDATO UART2_TxD PE26	O O IO	2mA, pullup-pe	SDATO: AC97/I2S serial data output UART2_TxD: UART 2 transmitting data PE26: GPIO group E bit 26	VDDIO

	WAIT_	I	2mA,	WAIT_: Slow static memory/device wait signal	
55	PC20	IO	pullup-pe	PC20: GPIO group C bit 20	VDDIO
	CIM_VSYN	I	2mA,	CIM_VSYN: CIM VSYNC input	
56	PE10	IO	pullup-pe	PE10: GPIO group E bit 10	VDDIO
	CIM_HSYN	I	2mA,	CIM_HSYN: CIM HSYNC input	
57	PE11	IO	pullup-pe	PE11: GPIO group E bit 11	VDDIO
	CIM_D0	I	2mA,	CIM_D0: CIM data input bit 0	
58	PE0	IO	pullup-pe	PE0: GPIO group E bit 0	VDDIO
	CIM_D1	I	2mA,	CIM_D1: CIM data input bit 1	
59	PE1	IO	pullup-pe	PE1: GPIO group E bit 1	VDDIO
	CIM_D2	I	2mA,	CIM_D2: CIM data input bit 2	
60	PE2	IO	pullup-pe	PE2: GPIO group E bit 2	VDDIO
	CIM_D3	I	2mA,	CIM_D3: CIM data input bit 3	
61	PE3	IO	pullup-pe	PE3: GPIO group E bit 3	VDDIO
	CIM_D4	I	2mA,	CIM_D4: CIM data input bit 4	
62	PE4	IO	pullup-pe	PE4: GPIO group E bit 4	VDDIO
	CIM_D5	I	2mA,	CIM_D5: CIM data input bit 5	
63	PE5	IO	pullup-pe	PE5: GPIO group E bit 5	VDDIO
	CIM_D6	I	2mA,	CIM_D6: CIM data input bit 6	
64	PE6	IO	pullup-pe	PE6: GPIO group E bit 6	VDDIO
	CIM_D7	I	2mA,	CIM_D7: CIM data input bit 7	
65	PE7	IO	pullup-pe	PE7: GPIO group E bit 7	VDDIO
	CIM_PCLK	I	2mA,	CIM_PCLK: CIM pixel clock input	
66	PE9	IO	pullup-pe	PE9: GPIO group E bit 9	VDDIO
	CIM_MCLK	I	4mA,	CIM_MCLK: CIM master clock output	
67	PE8	IO	pullup-pe	PE8: GPIO group E bit 8	VDDIO
				PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK	
	PWM2	O		clock	
	SCLK_RSTN	O	2mA,	SCLK_RSTN: I2S system clock output or AC97 reset output	
68	PE22	IO	pullup-pe	PE22: GPIO group E bit 22	VDDIO
		O		PWM3: PWM 3 output	
	PWM3BCLK	IO	2mA,	BCLK: AC97/I2S bit clock	
69	PE23	IO	pullup-pe	PE23: GPIO group E bit 23	VDDIO
	PWM4	O		PWM4: PWM 6 output	
	SYNC	IO	2mA,	SYNC: AC97 frame SYNC or I2S Left/Right	
70	PE24	IO	pullup-pe	PE24: GPIO group E bit 24	VDDIO
	PWM5	O		PWM5: PWM 7 output	
	OWI	IO	2mA,	OWI: One wire interface	
71	PE25	IO	pullup-pe	PE25: GPIO group E bit 25	VDDIO
	MSC0_D0	IO	4mA,	MSC0_D0: MSC (MMC/SD) 0 data bit 0	
72	PF0	IO	pullup-pe	PF0: GPIO group F bit 0	VDDIO
	MSC0_D1	IO	4mA,	MSC0_D1: MSC (MMC/SD) 0 data bit 1	
73	PF1	IO	pullup-pe	PF1: GPIO group F bit 1	VDDIO
	MSC0_D2	IO	4mA,	MSC0_D2: MSC (MMC/SD) 0 data bit 2	
74	DREQ	I	pullup-pe	DREQ: External DMA request input	VDDIO

	PF2	IO		PF2: GPIO group F bit 2	
	MSC0_D3	IO		MSC0_D3: MSC (MMC/SD) 0 data bit 3	
	DACK	O	4mA,	DACK: External DMA acknowledge output	
75	PF3	IO	pullup-pe	PF3: GPIO group F bit 3	VDDIO
	MSC0_D4	IO		MSC0_D4: MSC (MMC/SD) 0 data bit 4	
	UART0_RxD	I	4mA,	UART0_RxD: UART 0 Receiving data	
76	PF4	IO	pullup-pe	PF4: GPIO group F bit 4	VDDIO
	MSC0_D5	IO		MSC0_D5: MSC (MMC/SD) 0 data bit 5	
	UART0_TxD	O	4mA,	UART0_TxD: UART 0 transmitting data	
77	PF5	IO	pullup-pe	PF5: GPIO group F bit 5	VDDIO
	MSC0_D6	IO		MSC0_D6: MSC (MMC/SD) 0 data bit 6	
	UART0_CTS_	I	4mA,	UART0_CTS_: UART 0 CTS_ input	
78	PF6	IO	pullup-pe	PF6: GPIO group F bit 6	VDDIO
	MSC0_D7	IO		MSC0_D7: MSC (MMC/SD) 0 data bit 7	
	UART0_RTS_	O	4mA,	UART0_RTS_: UART 0 RTS_ output	
79	PF7	IO	pullup-pe	PF7: GPIO group F bit 7	VDDIO
	MSC0_CMD	IO	4mA,	MSC0_CMD: MSC (MMC/SD) 0 command	
80	PF9	IO	pullup-pe	PF9: GPIO group F bit 9	VDDIO
	MSC0_CLK	O	4mA,	MSC0_CLK: MSC (MMC/SD) 0 clock output	
81	PF8	IO	pullup-pe	PF8: GPIO group F bit 8	VDDIO
	TSCLK	I	2mA,	TSCLK: TS interface clock input	
82	PF20	IO	pullup-pe	PF20: GPIO group F bit 20	VDDIO
	TSFAIL	I	2mA,	TSFAIL: TS interface error package indicator input	
83	PF23	IO	pullup-pe	PF23: GPIO group F bit 23	VDDIO
	TSFRM	I	2mA,	TSFRM: TS interface frame valid input	
84	PF22	IO	pullup-pe	PF22: GPIO group F bit 22	VDDIO
	TSSTR	I	2mA,	TSSTR: TS interface frame start input	
85	PF21	IO	pullup-pe	PF21: GPIO group F bit 21	VDDIO
	SD8	IO		SD8: Static memory data bus bit 8	
	TSDI0	I	2mA,	TSDI0: TS interface input data bus bit 0	
86	PC8	IO	pullup-pe	PC8: GPIO group C bit 8	VDDIO
		IO		SD9: Static memory data bus bit 9	
	TSDI1	I	2mA,	TSDI1: TS interface input data bus bit 1	
87	PC9	IO	pullup-pe	PC9: GPIO group C bit 9	VDDIO
	SD10	IO		SD10: Static memory data bus bit 10	
	TSDI2	I	2mA,	TSDI2: TS interface input data bus bit 2	
88	PC10	IO	pullup-pe	PC10: GPIO group C bit 10	VDDIO
	SD11	IO		SD11: Static memory data bus bit 11	
	TSDI3	I	2mA,	TSDI3: TS interface input data bus bit 3	
89	PC11	IO	pullup-pe	PC11: GPIO group C bit 11	VDDIO
	SD12	IO		SD12: Static memory data bus bit 12	
	TSDI4	I	2mA,	TSDI4: TS interface input data bus bit 4	
90	PC12	IO	pullup-pe	PC12: GPIO group C bit 12	VDDIO

	SD13	IO		SD13: Static memory data bus bit 13	
	TSDI5	I	2mA,	TSDI5: TS interface input data bus bit 5	
91	PC13	IO	pullup-pe	PC13: GPIO group C bit 13	VDDIO
	SD14	IO		SD14: Static memory data bus bit 14	
	TSDI6	I	2mA,	TSDI6: TS interface input data bus bit 6	
92	PC14	IO	pullup-pe	PC14: GPIO group C bit 14	VDDIO
	SD15	IO		SD15: Static memory data bus bit 15	
	TSDI7	I	2mA,	TSDI7: TS interface input data bus bit 7	
93	PC15	IO	pullup-pe	PC15: GPIO group C bit 15	VDDIO
	CS1_	O	2mA,	CS1_: Static memory chip select 1	
94	PC21	IO	pullup-pe	PC21: GPIO group C bit 21	VDDIO
	CS2_	O	2mA,	CS2_: Static memory chip select 2	
95	PC22	IO	pullup-pe	PC22: GPIO group C bit 22	VDDIO
	CS3_	O	2mA,	CS3_: Static memory chip select 3	
96	PC23	IO	pullup-pe	PC23: GPIO group C bit 23	VDDIO
	CS4_	O	2mA,	CS4_: Static memory chip select 4	
97	PC24	IO	pullup-pe	PC24: GPIO group C bit 24	VDDIO
	A15_3	O		A15_3: Static memory address bus bit 15 or bit 3	
	CL	O	2mA,	CL: NAND flash command latch	
98	PB15	IO	pullup-pe	PB15: GPIO group B bit 15	VDDIO
	A16_4	O		A16_4: Static memory address bus bit 16 or bit 4	
	AL	O	2mA,	AL: NAND flash address latch	
99	PC16	IO	pullup-pe	PC16: GPIO group C bit 16	VDDIO
				PC27: GPIO group C bit 27. If NAND flash is used, it should connect	
			2mA,	to NAND	
100	PC27 (FRB)	IO	pullup-pe	FRB (NAND flash ready/busy)	VDDIO
	FRE_	O	2mA,	FRE_: NAND flash read enable	
101	PC28	IO	pullup-pe	PC28: GPIO group C bit 28	VDDIO
	FWE_	O	2mA,	FWE_: NAND flash write enable	
102	PC29	IO	pullup-pe	PC29: GPIO group C bit 29	VDDIO
	WR_	O	2mA,	WR_: Static memory write strobe	
103	PC26	IO	pullup-pe	PC26: GPIO group C bit 26	VDDIO
	RD_	O	2mA,	RD_: Static memory read strobe	
104	PC25	IO	pullup-pe	PC25: GPIO group C bit 25	VDDIO
	SA2	O		SA2: Static memory address bus bit 2	
	A19	O	2mA,	A19: Static memory address bus bit 19	
105	PC19	IO	pullup-pe	PC19: GPIO group C bit 19, sometimes output only[3]	VDDIO
	SA1	O		SA1: Static memory address bus bit 1	
	A18	O	2mA,	A18: Static memory address bus bit 18	
106	PC18	IO	pullup-pe	PC18: GPIO group C bit 18, sometimes output only[3]	VDDIO
	SA0	O		SA0: Static memory address bus bit 0	
	A17	O	2mA,	A17: Static memory address bus bit 17	
107	PC17	O	pullup-pe	PC17: GPIO group C bit 17	VDDIO
	SD7	IO	4mA,	SD7: Static memory data bus bit 7	
108	PC7	IO	pullup-pe	PC7: GPIO group C bit 7	VDDIO

	SD6	IO	4mA,	SD6: Static memory data bus bit 6	
109	PC6	IO	pullup-pe	PC6: GPIO group C bit 6	VDDIO
	SD5	IO		SD5: Static memory data bus bit 5	
	A25	O	4mA,	A25: Static memory address bus bit 5	
110	PC5	IO	pullup-pe	PC5: GPIO group C bit 5	VDDIO
	SD4	IO		SD4: Static memory data bus bit 4	
	A24	O	4mA,	A24: Static memory address bus bit 4	
111	PC4	IO	pullup-pe	PC4: GPIO group C bit 4	VDDIO
	SD3	IO		SD3: Static memory data bus bit 3	
	A23	O	4mA,	A23: Static memory address bus bit 3	
112	PC3	IO	pullup-pe	PC3: GPIO group C bit 3	VDDIO
	SD2	IO		SD2: Static memory data bus bit 2	
	A22	O	4mA,	A22: Static memory address bus bit 2	
113	PC2	IO	pullup-pe	PC2: GPIO group C bit 2	VDDIO
	SD1	IO		SD1: Static memory data bus bit 1	
	A21	O	4mA,	A21: Static memory address bus bit 1	
114	PC1	IO	pullup-pe	PC1: GPIO group C bit 1	VDDIO
	SD0	IO		SD0: Static memory data bus bit 0	
	A20	O	4mA,	A20: Static memory address bus bit 0	
115	PC0	IO	pullup-pe	PC0: GPIO group C bit 0	VDDIO
116	SDRAM_VDD	P		power, 3.3V	-
117	SDRAM_VDD	P		power, 3.3V	-
118	SDRAM_GND	P		power, ground	-
119	SDRAM_GND	P		power, ground	-
				SDWE_: SDRAM write enable	
	SDWE_ &			BUFD_: Select CPU to SRAM chip direction in data bi-direction	
	BUFD_	O	12mA,	buffer	
120	PB19	IO	pullup-pe	PB19: GPIO group B bit 19	VDDIOL
	A14	O	12mA,	A14: SDRAM/Static memory address bus bit 14	
121	PB14	IO	pullup-pe	PB14: GPIO group B bit 14	VDDIOL
	A13	O	12mA,	A13: SDRAM/Static memory address bus bit 13	
122	PB13	IO	pullup-pe	PB13: GPIO group B bit 13	VDDIOL
	A12	O	12mA,	A12: SDRAM/Static memory address bus bit 12	
123	PB12	IO	pullup-pe	PB12: GPIO group B bit 12	VDDIOL
	A11	O	12mA,	A11: SDRAM/Static memory address bus bit 11	
124	PB11	IO	pullup-pe	PB11: GPIO group B bit 11	VDDIOL
	A10	O	12mA,	A10: SDRAM/Static memory address bus bit 10	
125	PB10	IO	pullup-pe	PB10: GPIO group B bit 10	VDDIOL
	A9	O	12mA,	A9: SDRAM/Static memory address bus bit 9	
126	PB9	IO	pullup-pe	PB9: GPIO group B bit 9	VDDIOL
	A8	O	12mA,	A8: SDRAM/Static memory address bus bit 8	
127	PB8	IO	pullup-pe	PB8: GPIO group B bit 8	VDDIOL
	A7	O	12mA,	A7: SDRAM/Static memory address bus bit 7	
128	PB7	IO	pullup-pe	PB7: GPIO group B bit 7	VDDIOL
129	A6	O	12mA,	A6: SDRAM/Static memory address bus bit 6	VDDIOL

	PB6	IO	pullup-pe	PB6: GPIO group B bit 6	
	A5	O	12mA,	A5: SDRAM/Static memory address bus bit 5	
130	PB5	IO	pullup-pe	PB5: GPIO group B bit 5	VDDIOL
	A4	O	12mA,	A4: SDRAM/Static memory address bus bit 4	
131	PB4	IO	pullup-pe	PB4: GPIO group B bit 4	VDDIOL
	A3	O	12mA,	A3: SDRAM/Static memory address bus bit 3	
132	PB3	IO	pullup-pe	PB3: GPIO group B bit 3	VDDIOL
	A2	O	12mA,	A2: SDRAM/Static memory address bus bit 2	
133	PB2	IO	pullup-pe	PB2: GPIO group B bit 2	VDDIOL
	A1	O	12mA,	A1: SDRAM/Static memory address bus bit 1	
134	PB1	IO	pullup-pe	PB1: GPIO group B bit 1	VDDIOL
	A0	O	12mA,	A0: SDRAM/Static memory address bus bit 0	
135	PB0	IO	pullup-pe	PB0: GPIO group B bit 0	VDDIOL
	D8	IO	8mA,	D8: SDRAM data bus bit 8, static memory data bus bit 8	
136	PA8	IO	pullup-pe	PA8: GPIO group A bit 8	VDDIOL
	D9	IO	8mA,	D9: SDRAM data bus bit 9, static memory data bus bit 9	
137	PA9	IO	pullup-pe	PA9: GPIO group A bit 9	VDDIOL
	D10	IO	8mA,	D10: SDRAM data bus bit 10, static memory data bus bit 10	
138	PA10	IO	pullup-pe	PA10: GPIO group A bit 10	VDDIOL
	D11	IO	8mA,	D11: SDRAM data bus bit 11, static memory data bus bit 11	
139	PA11	IO	pullup-pe	PA11: GPIO group A bit 11	VDDIOL
	D12	IO	8mA,	D12: SDRAM data bus bit 12, static memory data bus bit 12	
140	PA12	IO	pullup-pe	PA12: GPIO group A bit 12	VDDIOL
	D13	IO	8mA,	D13: SDRAM data bus bit 13, static memory data bus bit 13	
141	PA13	IO	pullup-pe	PA13: GPIO group A bit 13	VDDIOL
	D14	IO	8mA,	D14: SDRAM data bus bit 14, static memory data bus bit 14	
142	PA14	IO	pullup-pe	PA14: GPIO group A bit 14	VDDIOL
	D15	IO	8mA,	D15: SDRAM data bus bit 15, static memory data bus bit 15	
143	PA15	IO	pullup-pe	PA15: GPIO group A bit 15	VDDIOL
	D0	IO	12mA,	D0: SDRAM data bus bit 0, static memory data bus bit 0	
144	PA0	IO	pullup-pe	PA0: GPIO group A bit 0	VDDIOL
	D1	IO	12mA,	D1: SDRAM data bus bit 1, static memory data bus bit 1	
145	PA1	IO	pullup-pe	PA1: GPIO group A bit 1	VDDIOL
	D2	IO	12mA,	D2: SDRAM data bus bit 2, static memory data bus bit 2	
146	PA2	IO	pullup-pe	PA2: GPIO group A bit 2	VDDIOL
	D3	IO	12mA,	D3: SDRAM data bus bit 3, static memory data bus bit 3	
147	PA3	IO	pullup-pe	PA3: GPIO group A bit 3	VDDIOL
	D4	IO	12mA,	D4: SDRAM data bus bit 4, static memory data bus bit 4	
148	PA4	IO	pullup-pe	PA4: GPIO group A bit 4	VDDIOL
	D5	IO	12mA,	D5: SDRAM data bus bit 5, static memory data bus bit 5	
149	PA5	IO	pullup-pe	PA5: GPIO group A bit 5	VDDIOL
	D6	IO	12mA,	D6: SDRAM data bus bit 6, static memory data bus bit 6	
150	PA6	IO	pullup-pe	PA6: GPIO group A bit 6	VDDIOL
	D7	IO	12mA,	D7: SDRAM data bus bit 7, static memory data bus bit 7	
151	PA7	IO	pullup-pe	PA7: GPIO group A bit 7	VDDIOL

	MSC1_D3	IO	4mA,	MSC1_D3: MSC (MMC/SD) 1 data bit 3	
152	PF13	IO	pullup-pe	PF13: GPIO group F bit 13	VDDIO
	MSC1_D2	IO	4mA,	MSC1_D2: MSC (MMC/SD) 1 data bit 2	
153	PF12	IO	pullup-pe	PF12: GPIO group F bit 12	VDDIO
	MSC1_D1	IO	4mA,	MSC1_D1: MSC (MMC/SD) 1 data bit 1	
154	PF11	IO	pullup-pe	PF11: GPIO group F bit 11	VDDIO
	MSC1_D0	IO	4mA,	MSC1_D0: MSC (MMC/SD) 1 data bit 0	
155	PF10	IO	pullup-pe	PF10: GPIO group F bit 10	VDDIO
	MSC1_CMD	IO	4mA,	MSC1_CMD: MSC (MMC/SD) 1 command	
156	PF15	IO	pullup-pe	PF15: GPIO group F bit 15	VDDIO
	MSC1_CLK	O	4mA,	MSC1_CLK: MSC (MMC/SD) 1 clock output	
157	PF14	IO	pullup-pe	PF14: GPIO group F bit 14	VDDIO
	SSI1_DT	O	4mA,	SSI1_DT: SSI 1 data output	
158	PD27	IO	pullup-pe	PD27: GPIO group D bit 27	VDDIO
	SSI1_DR	I	4mA,	SSI1_DR: SSI 1 data input	
159	PD28	IO	pullup-pe	PD28: GPIO group D bit 28	VDDIO
	SSI1_CE1_	O	4mA,	SSI1_CE1_: SSI 1 chip enable 1	
160	PD30	IO	pullup-pe	PD30: GPIO group D bit 30	VDDIO
	SSI1_CE0_	O	4mA,	SSI1_CE0_: SSI 1 chip enable 0	
161	PD29	IO	pullup-pe	PD29: GPIO group D bit 29	VDDIO
	SSI1_CLK	O	4mA,	SSI1_CLK: SSI 1 clock output	
162	PD26	IO	pullup-pe	PD26: GPIO group D bit 26	VDDIO
	UART3_CTS_	I		UART3_CTS_: UART 3 CTS_ input	
	LCD_D_R0	O	4mA,	LCD_D_R0: Red data bit 0, used in 24-bit data bus	
163	PF18	IO	pullup-pe	PF18: GPIO group F bit 18	VDDIO
	UART3_RTS_	O		UART3_RTS_: UART 3 RTS_ output	
	LCD_D_B0	O	4mA,	LCD_D_B0: Blue data bit 0, used in 24-bit data bus	
164	PF19	IO	pullup-pe	PF19: GPIO group F bit 19	VDDIO
	UART3_TxD	O	2mA,	UART3_TxD: UART 3 transmitting data	
165	PF17	IO	pullup-pe	PF17: GPIO group F bit 17	VDDIO
	UART3_RxD	I	2mA,	UART3_RxD: UART 3 Receiving data	
166	PF16	IO	pullup-pe	PF16: GPIO group F bit 16	VDDIO
	LCD_SPL	O		LCD_SPL: LCD SPL output	
	LCD_D_G0	O	4mA,	LCD_D_G0: Green data bit 0, used in 24-bit data bus	
167	PD23	IO	pullup-pe	PD23: GPIO group D bit 23	VDDIO
	LCD_CLS	O		LCD_CLS: LCD CLS output	
	LCD_D_R1	O	4mA,	LCD_D_R1: Red data bit 1, used in 24-bit data bus	
168	PD22	IO	pullup-pe	PD22: GPIO group D bit 22	VDDIO
	LCD_PS	O		LCD_PS: LCD PS output for special TFT	
	LCD_D_G1	O	4mA,	LCD_D_G1: Green data bit 1, used in 24-bit data bus	
169	PD24	IO	pullup-pe	PD24: GPIO group D bit 24	VDDIO
	LCD_REV	O		LCD_REV: LCD REV output for special TFT	
	LCD_D_B1	O	4mA,	LCD_D_B1: Blue data bit 1, used in 24-bit data bus	
170	PD25	IO	pullup-pe	PD25: GPIO group D bit 25	VDDIO
171	LCD_DE	O	4mA,	LCD_DE: STN AC bias drive/non-STN data enable	VDDIO

	PD21	IO	pullup-pe	PD21: GPIO group D bit 21	
172	LCD_VSYN PD20	IO IO	4mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PD20: GPIO group D bit 20	VDDIO
173	LCD_HSYN PD19	IO IO	4mA, pullup-pe	LCD_HSYN: LCD line clock/horizonal sync PD19: GPIO group D bit 19	VDDIO
174	LCD_PCLK PD18	IO IO	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PD18: GPIO group D bit 18	VDDIO
175	LCD_D17 PD17	O IO	4mA, pullup-pe	LCD_D17: LCD data bus bit 17 PD17: GPIO group D bit 17	VDDIO
176	LCD_D16 PD16	O IO	4mA, pullup-pe	LCD_D16: LCD data bus bit 16 PD16: GPIO group D bit 16	VDDIO
177	LCD_D15 PD15	O IO	4mA, pullup-pe	LCD_D15: LCD data bus bit 15 PD15: GPIO group D bit 15	VDDIO
178	LCD_D14 PD14	O IO	4mA, pullup-pe	LCD_D14: LCD data bus bit 14 PD14: GPIO group D bit 14	VDDIO
179	LCD_D13 PD13	O IO	4mA, pullup-pe	LCD_D13: LCD data bus bit 13 PD13: GPIO group D bit 13	VDDIO
180	LCD_D12 PD12	O IO	4mA, pullup-pe	LCD_D12: LCD data bus bit 12 PD12: GPIO group D bit 12	VDDIO
181	LCD_D11 PD11	O IO	4mA, pullup-pe	LCD_D11: LCD data bus bit 11 PD11: GPIO group D bit 11	VDDIO
182	LCD_D10 PD10	O IO	4mA, pullup-pe	LCD_D10: LCD data bus bit 10 PD10: GPIO group D bit 10	VDDIO
183	LCD_D9 PD9	O IO	4mA, pullup-pe	LCD_D9: LCD data bus bit 9 PD9: GPIO group D bit 9	VDDIO
184	LCD_D8 PD8	O IO	4mA, pullup-pe	LCD_D8: LCD data bus bit 8 PD8: GPIO group D bit 8	VDDIO
185	LCD_D7 PD7	O IO	4mA, pullup-pe	LCD_D7: LCD data bus bit 7 PD7: GPIO group D bit 7	VDDIO
186	LCD_D6 PD6	O IO	4mA, pullup-pe	LCD_D6: LCD data bus bit 6 PD6: GPIO group D bit 6	VDDIO
187	LCD_D5 PD5	O IO	4mA, pullup-pe	LCD_D5: LCD data bus bit 5 PD5: GPIO group D bit 5	VDDIO
188	LCD_D4 PD4	O IO	4mA, pullup-pe	LCD_D4: LCD data bus bit 4 PD4: GPIO group D bit 4	VDDIO
189	LCD_D3 PD3	O IO	4mA, pullup-pe	LCD_D3: LCD data bus bit 3 PD3: GPIO group D bit 3	VDDIO
190	LCD_D2 PD2	O IO	4mA, pullup-pe	LCD_D2: LCD data bus bit 2 PD2: GPIO group D bit 2	VDDIO
191	LCD_D1 PD1	O IO	4mA, pullup-pe	LCD_D1: LCD data bus bit 1 PD1: GPIO group D bit 1	VDDIO
192	LCD_D0 PD0	O IO	4mA, pullup-pe	LCD_D0: LCD data bus bit 0 PD0: GPIO group D bit 0	VDDIO
193	I2C_SCK	IO	4mA,	I2C_SCK: I2C serial clock	VDDIO

	PE13	IO	pullup-pe	PE13: GPIO group E bit 13	
194	I2C_SDA PE12	IO IO	4mA, pullup-pe	I2C_SDA: I2C serial data PE12: GPIO group E bit 12	VDDIO
195	VDDDAC	P		AVDDA: Power supply for LUMA and CHROMA output, 3.3 V (IO1:AVD33R, IO2:AVD33G, IO3:AVDD, VDWELL)	-
196	GND	P		AVSDA: Ground for LUMA and CHROMA output (IO1/IO2: AVS33R, AVS33G, AVSS, VSSUB)	-
197	CHROMA	AO		CHROMA: DAC analog output Chrominance of S-Video	VDDDAC
198	LUMA	AO		LUMA: DAC analog output for CVBS or luminance of S-Video	VDDDAC
199	BOOT_SEL0 PC30	I O	2mA, Schmitt	BOOT_SEL0: Boot select bit 0 PC30: GPIO group C bit 30, reset to BOOT_SEL0	VDDIO
200	BOOT_SEL1 PC31	I IO	2mA, Schmitt	BOOT_SEL1: Boot select bit 1 PC31: GPIO group C bit 31, reset to BOOT_SEL1, reset to BOOT_SEL1	VDDIO
201	UART1_TxD PE17	O IO	2mA, pullup-pe	UART1_TxD: UART 1 transmitting data PE17: GPIO group E bit 17	VDDIO
202	UART1_RxD PE16	I IO	2mA, pullup-pe	UART1_RxD: UART 1 Receiving data PE16: GPIO group E bit 16	VDDIO

Notes:

[1]. The meaning of phases in IO cell characteristics are

a) 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12mA

b) Pull-up: The IO cell contains a pull-up resistor

c) Pull-down: The IO cell contains a pull-down resistor

d) Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or

disabled by setting corresponding register.

e) Schmitt: The IO cell is Schmitt trig input

[2]. For any GPIO shared pin except WAIT_/PC27 and CKO/PB24, the reset state is GPIO input

with internal pull-up. The WAIT_/PC27 and CKO/PB24 are initialed to WAIT_ and CKO functions

with internal pull-up.

[3]. PC18/PC19 are sometimes used to decide the EXCLK frequency for USB boot. In this case they

should be used as output only GPIO. Resisters may need to pull up/down these pins to tell

which EXCLK is. Please reference to 3.6.3 for the details.

有关 GPIO 更多的内容请参看官方 Jz4750_ds.pdf。

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